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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,214	07/08/2003	William W. Brown	10030275-1	9777

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EXAMINER
DSOUZA, JOSEPH FRANCIS A

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,214	BROWN, WILLIAM W.	
	Examiner	Art Unit	
	Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-12* is/are allowed.

6)☒ Claim(s) *1,2,4-6,8,9,13-14,16 and 17* is/are rejected.

7)☒ Claim(s) *3,7 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

1. The disclosure is objected to because of the following informalities: On page 2, line 10, "...first threshold and less than the first threshold" should be changed to "... first threshold and less than the third threshold".

Appropriate correction is required.

Claim Objections

2. Claims 1,6,10 and 13 are objected to because of the following informalities: The preamble of claims 1, 6 and 10 should be changed to "A data slicer for... comprising:". The preamble of claim 13 should be changed to "An integrated circuit for... comprising:". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 – 2, 4, 6, 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki et al. (US 20030108092) in view of Patel et al. (US 6.313.885).

Regarding claim 1, Gorecki discloses a data slicer comprising:

a first comparator circuit that establishes a first threshold; a second comparator circuit that establishes a second threshold; and a third comparator circuit that establishes a third threshold; wherein the second threshold is greater than the first threshold and less than the third threshold, wherein each of the comparator circuits has an offset, and wherein the first and third comparator circuits have symmetrical offsets (page 8, paragraph 70; wherein the first, second and third thresholds are the values –2,0,+2 respectively and the offsets are interpreted as the values –2,0 and +2 values and the symmetrical offsets are –1 and + 2).

Gorecki does not explicitly disclose a comparator circuit for the slicer.

In the same field of endeavor, however, Patel discloses a comparator circuit (column 11, lines 38 – 61).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the comparator, as taught by Patel, in the system of Gorecki because this would allow the input symbol to be compared with the threshold to obtain the correct output symbol, as is well known in the art.

Regarding claim 2, Gorecki discloses symmetrical offsets (page 8, paragraph 70).

Gorecki does not explicitly disclose how the symmetrical offsets are provided.

In the same field of endeavor, however, Patel discloses the first and third comparator circuits have output circuits providing the symmetrical offsets (Fig. 2, element 100; column 11, lines 38 – 61; wherein the symmetrical values are provided by the bin amplitude comparator).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the symmetrical threshold values, as taught by Patel, in the system of Gorecki because this would allow the input symbol to be compared with the thresholds to obtain the correct output symbol, as is well known in the art.

Regarding claim 4, Gorecki discloses the first and third thresholds are equally spaced from the second threshold (page 8, paragraph 70; wherein the first, second and third thresholds are the values –2,0,+2 respectively resulting in a spacing of 2 from the center threshold).

Claim 6, 8 are similarly analyzed as claim 1, 4 respectively.

5. Claim 5, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki et al. (US 20030108092) in view of Patel et al. (US 6.313.885) and further in view of Reymond (US 5,517, 532).

Regarding claim 5, Gorecki does not disclose that the comparator circuits are in CMOS.

In the same field of endeavor, however, Reymond discloses the comparator circuits are formed from complimentary metal oxide semiconductor devices (column 11, lines 2 - 5).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Reymond, in the system of Gorecki because this would allow the benefits of CMOS, namely low power consumption and high level of integration, to be utilized.

Claim 9 is similarly analyzed as claim 5.

6. Claim 13, 14, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki et al. (US 20030108092) in view of Patel et al. (US 6.313.885) and further in view of Measor et al. (US 5,699,386).

Regarding claim 13, Gorecki discloses a data slicer including, a first comparator circuit that establishes a first threshold, a second comparator circuit that establishes a second

threshold, and a third comparator circuit that establishes a third threshold, wherein the second threshold is greater than the first threshold and less than the third threshold, wherein each of the comparator circuits has an offset, and wherein the first and third comparator circuits have symmetrical offsets (page 8, paragraph 70; wherein the first, second and third thresholds are the values –2,0,+2 respectively and the offsets are interpreted as the values –2,0 and +2 values and the symmetrical offsets are –1 and + 2).

Gorecki does not explicitly disclose a comparator circuit for the slicer, that the slicer is implemented on an integrated circuit comprising a substrate of semiconductor material.

In the same field of endeavor, however, Patel discloses a comparator circuit (column 11, lines 38 – 61).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the comparator, as taught by Patel, in the system of Gorecki because this would allow the input symbol to be compared with the threshold to obtain the correct output symbol, as is well known in the art.

In the same field of endeavor, however, Measor discloses an integrated circuit comprising: a substrate of semiconductor material; and a data slicer formed in the semiconductor material (column 3, lines 25 – 27, 41 - 46).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the comparator, as taught by Measor, in the system of Gorecki because this would allow the benefits of integrate circuits, small size, low power consumption etc, to be utilized, as is well known in the art.

Regarding claim 14, Gorecki discloses symmetrical offsets (page 8, paragraph 70).

Gorecki does not explicitly disclose how the symmetrical offsets are provided.

In the same field of endeavor, however, Patel discloses the first and third comparator circuits have output circuits providing the symmetrical offsets (Fig. 2, element 100; column 11, lines 38 – 61; wherein the symmetrical values are provided by the bin amplitude comparator).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the symmetrical threshold values, as taught by Patel, in the system of Gorecki because this would allow the input symbol to be compared with the thresholds to obtain the correct output symbol, as is well known in the art.

Regarding claim 16, Gorecki discloses the first and third thresholds are equally spaced from the second threshold (page 8, paragraph 70; wherein the first, second and third

thresholds are the values –2,0,+2 respectively resulting in a spacing of 2 from the center threshold).

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gorecki et al. (US 20030108092) in view of Patel et al. (US 6.313.885) and further in view of Measor et al. (US 5,699,386) and Reymond (US 5,517, 532).

Regarding claim 17, Gorecki does not disclose that the comparator circuits are in CMOS.

In the same field of endeavor, however, Reymond discloses the comparator circuits are formed from complimentary metal oxide semiconductor devices (column 11, lines 2 - 5).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Reymond, in the system of Gorecki because this would allow the benefits of CMOS, namely low power consumption and high level of integration, to be utilized.

Allowable Subject Matter

8. Claims 10 – 12 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to show that the load resistor center tap of the first comparator circuit is coupled to the load resistor center tap of the third comparator circuit (in Claim 10).

9. Claims 3, 7 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to PAM-4 signals and slicers:

Agazzi et al. (US 20020080898) discloses methods and systems for DSP-based receivers that utilize PAM-4 signals and slicers.

Trans et al. (US 20030016770) discloses a Channel equalization system and method that uses M-PAM.

Gorecki et al. (US 20030035497) discloses a System and method for providing slicer level adaptation.

Stonick et al. (US 20030108134) discloses a Method and apparatus for encoding and decoding digital communications data that uses PAM-n signals.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER